CLAIMS

What is claimed is:

1. A method comprising:

checking a current clock period when a memory is accessed, the current clock period being one of a given number of clock periods; and

setting a usage bit corresponding to the current clock period, the usage bit indicating usage information for the memory.

2. The method of claim 1, further comprising:

erasing usage bits corresponding to a new clock period when the new clock period begins.

3. The method of claim 2, wherein erasing the usage bits at once.

4. The method of claim 1, further comprising:

resetting usage bits when an address/tag of the memory is changed; and

setting a usage bit corresponding to a current clock period.

5. The method of claim 1, wherein the memory is a non-volatile cache memory.

6. The method of claim 5, wherein the given number of clock periods is four.

7. The method of claim 6, wherein one clock period is a plurality of hours.

8. The method of claim 5, wherein the non-volatile cache memory is a destructive read memory.

9. The method of claim 8, wherein the destructive read memory is one of a polymer ferroelectric RAM, a magnetic RAM or a core memory.

10. The method of claim 8, wherein setting the usage bit during a writeback cycle.

11. The method of claim 1, further comprising:

de-allocating data in the memory based upon the usage bits if the memory is considered full.

12. A memory comprising:

an area to store data; and

an area to store metadata for the data, the metadata including:

a plurality of usage bits to indicate usage information for the memory, each usage bit corresponding to one of a given number of clock periods.

13. The memory of claim 12, wherein the usage information is a least recently used information.

14. The memory of claim 12, wherein the memory is a non-volatile cache memory.

15. The memory of claim 14, wherein the given number of clock periods is four.

16. The memory of claim 14, wherein the non-volatile cache memory is a destructive read memory.

17. The memory of claim 16, wherein the destructive read memory is one of a polymer ferroelectric RAM, a magnetic RAM or a core memory.

18. A system comprising:

a memory to store data and metadata for the data, the metadata including a plurality of usage bits to indicate usage information for the memory, each usage bit corresponding to one of a given number of clock periods; and

a memory controller to update the usage bits based on the clock period and to de-allocate the data using the plurality of usage bits.

19. The system of claim 18, wherein the usage information is a least recently used information.

20. The system of claim 18, wherein the memory is a non-volatile cache memory.

21. The system of claim 20, wherein the given number of clock periods is four.

22. The system of claim 20, wherein the non-volatile cache memory is a destructive read memory.

23. A method comprising:

storing metadata indicating usage information for a memory; and

updating the metadata during a writeback cycle.

24. The method of claim 23, wherein the usage information is a least recently used information.

25. The method of claim 23, wherein storing usage bits as the metadata to indicate the usage information.

26. The method of claim 25, wherein updating the metadata comprises:

checking a current clock period when the memory is accessed, the current clock period being one of a predetermined number of clock periods; and

setting a usage bit corresponding to the current clock period, the usage bit indicating usage information for the memory.

27. The method of claim 26, wherein updating the metadata further comprises:

erasing usage bits corresponding to a new clock period when the new clock period begins.

28. The method of claim 26, wherein updating the metadata further comprises:

resetting usage bits when an address/tag of the memory is changed; and

setting a usage bit corresponding to a current clock period.

29. The method of claim 26, wherein the memory is a non-volatile cache memory.

30. The method of claim 29, wherein the predetermined number of clock periods is four.

31. The method of claim 29, wherein the non-volatile cache memory is a destructive read memory.

32. An instruction loaded in a machine readable medium comprising:

a first group of instructions to check a current clock period when a memory is accessed, the current clock period being one of a predetermined number of clock periods; and

a second group of instructions to set a usage bit corresponding to the current clock period, the usage bit indicating usage information for the memory.

33. The instruction of claim 32, further comprising:

a third group of instructions to erase usage bits corresponding to a new clock period when the new clock period begins.

34. The instruction of claim 32, further comprising:

a third group of instructions to reset usage bits for the memory when an address/tag of the memory is changed, and to set a usage bit corresponding to a current clock period.

35. An instruction loaded in a machine readable medium comprising:

a first group of instructions to store metadata information for a line of a memory; and

a second group of computer instructions to update the metadata during a writeback cycle.

36. The instruction of claim 35, wherein the first group of computer instructions to store metadata to indicate usage information for a line of a memory.

37. The instruction of claim 35, wherein the first group of computer instructions to store metadata for a line of a destructive read memory

38. A method comprising:

storing metadata for a cache memory; and

updating the metadata during a writeback cycle.

39. The method of claim 38, wherein the metadata is metadata indicating usage information for the cache memory.

40. The method of claim 38, wherein the cache memory is a non-volatile cache memory.

41. The method of claim 38, wherein the cache memory is a destructive read memory.